A Power Management IC with Bi-Directional Current-Mode Control and Partial Power Processing for Concentrating-PV Systems

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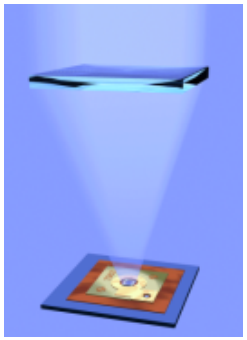
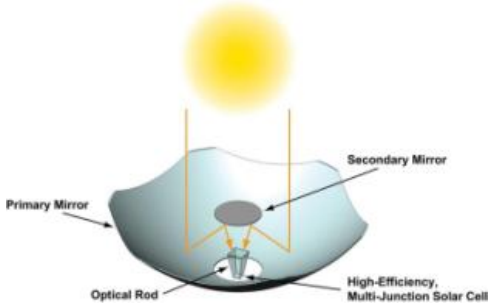
Introduction to CPV

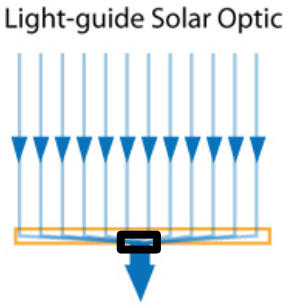
- **Concentrating-PV (CPV) systems**
  - High-efficiency multi-junction cells with wide spectral range
  - 500-1000X less semiconductor material
  - Low-cost optical concentrators
- Operated in near-uniform conditions
  - Two-axis mechanical tracking for consistent irradiation
  - Maximum Power Point Tracking (MPPT)



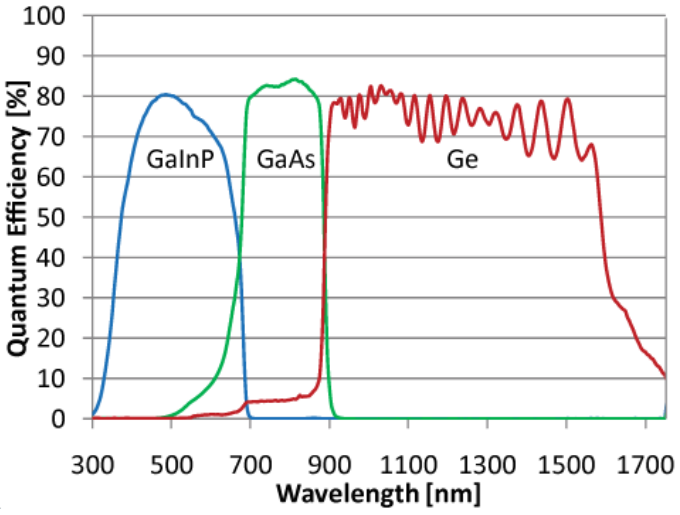
Soitec
http://www.soitec.com



SolFocus
http://www.solfocus.com

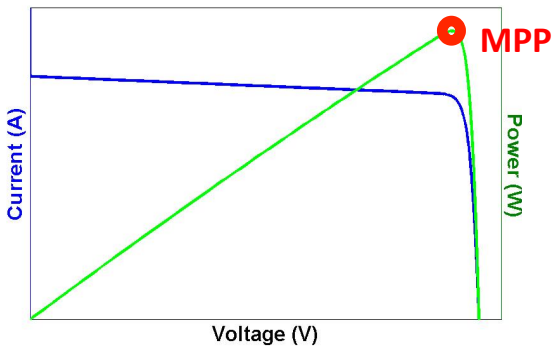


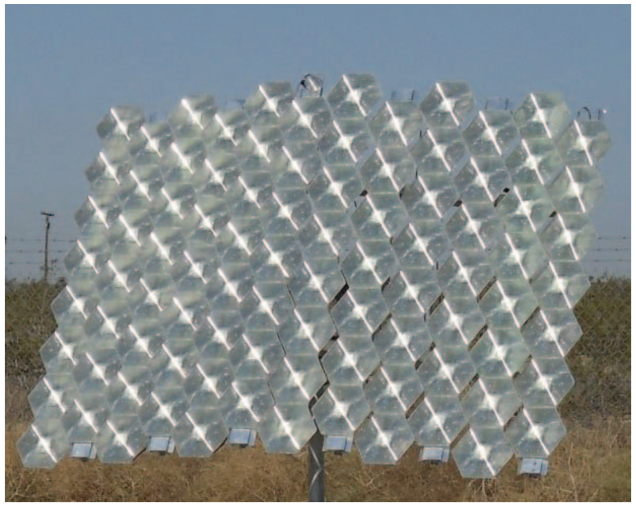
Morgan Solar
http://www.morgansolar.com
(targeted in this work)



Spectral Response of a Triple-Junction Cell

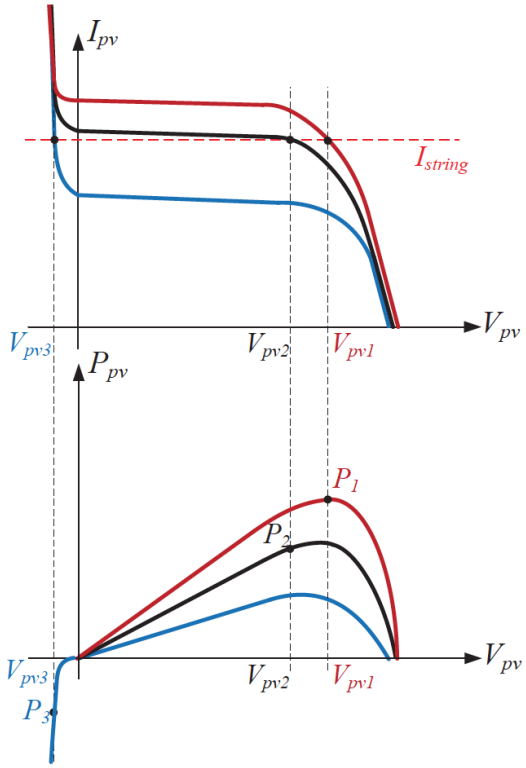
A typical PV I/V curve

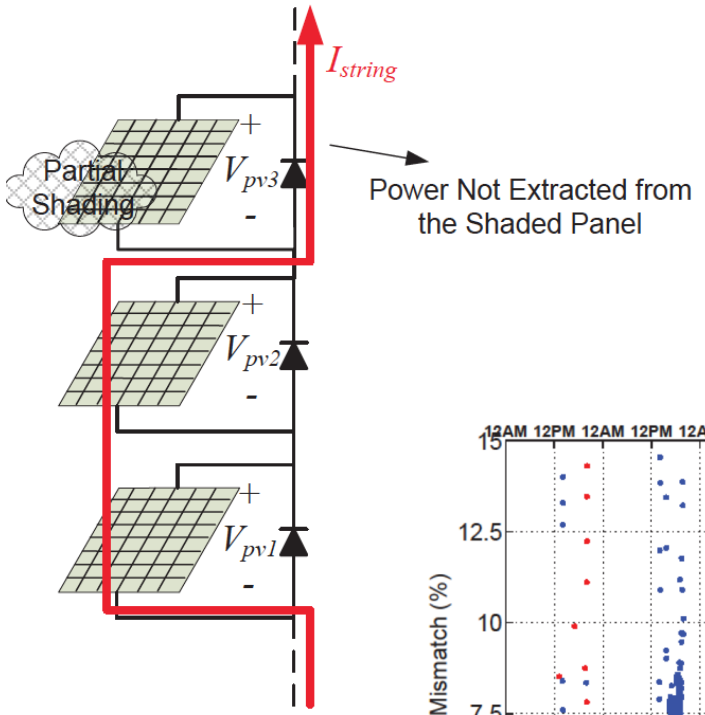




A CPV system by Morgan Solar

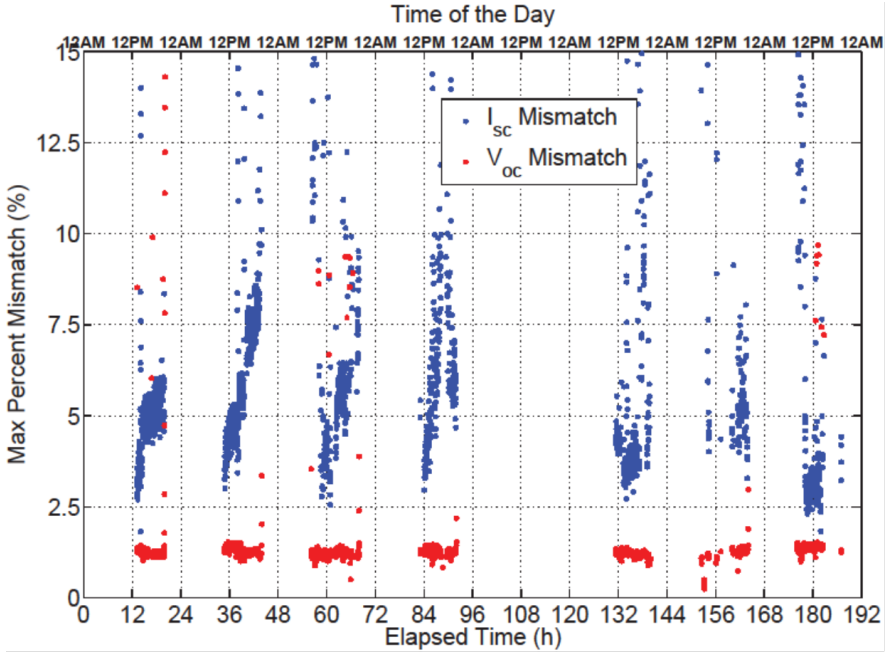
Mismatches in PV Systems





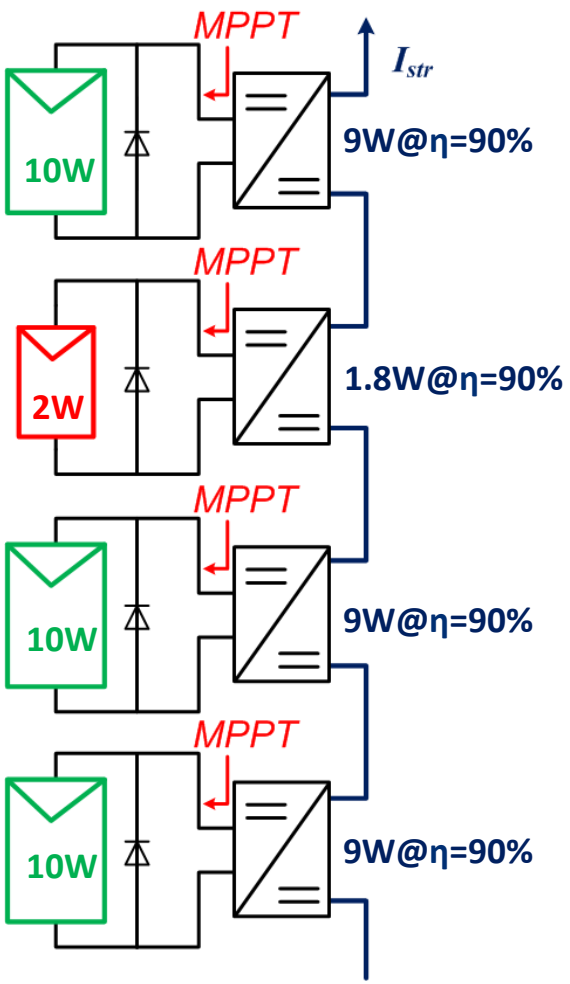
- Other mismatched conditions:
  - Cell electrical/thermal variations
  - Non-uniform aging
  - Concentrator misalignment
  - Non-uniform optical characteristics

- Under mismatched conditions, such as partial shading, some cells do not operate at their respective MPP.
- Power degradation due to partial shading also exists in CPV systems.



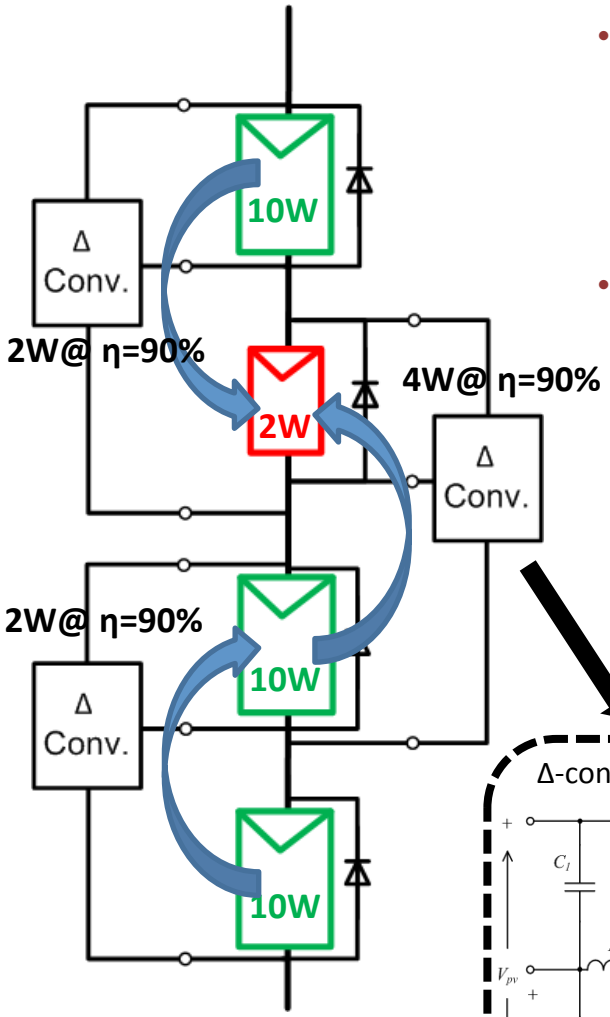
Measured mismatches in a 6-cell CPV system.
Observation: current mismatch > voltage mismatch.

Distributed MPPT vs. Δ-Conversion



DMPPT

P_{out} = 28.8W

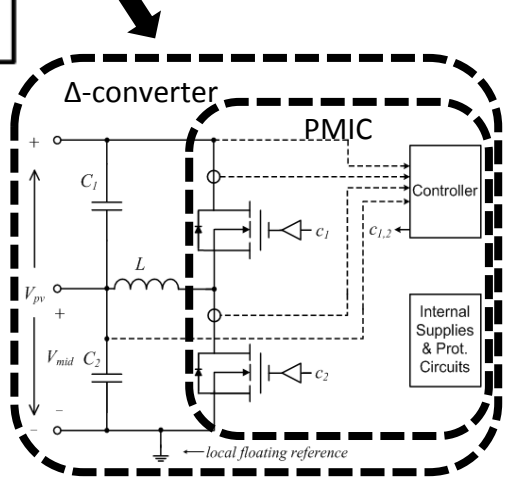


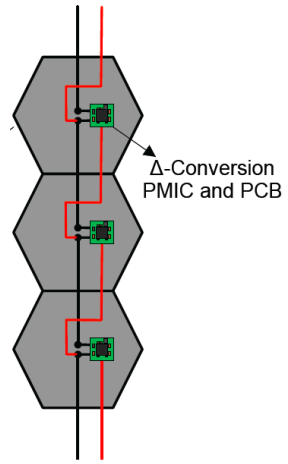
Δ-Conversion

(this work)

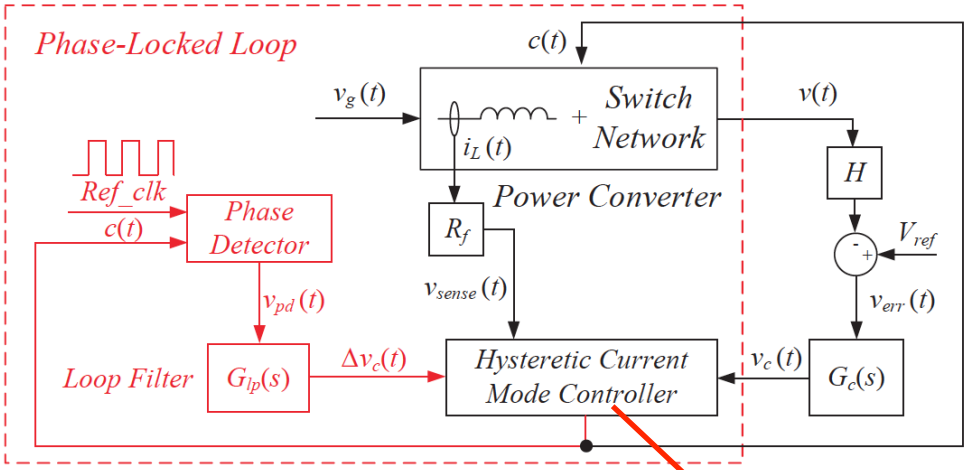
P_{out} = 31.2W

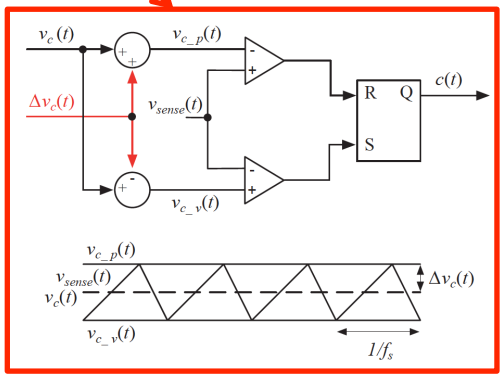
- DMPPT:
  - Converter handles full cell power.
  - Cost-prohibitive for cell-level CPV application.
  - Higher overall loss.
- Δ-Conversion:
  - Converter equalizes cell voltage of the two neighbouring cells.
  - Lower overall loss compared to DMPPT.
  - Converter handles partial cell power (lower power and cost requirement).



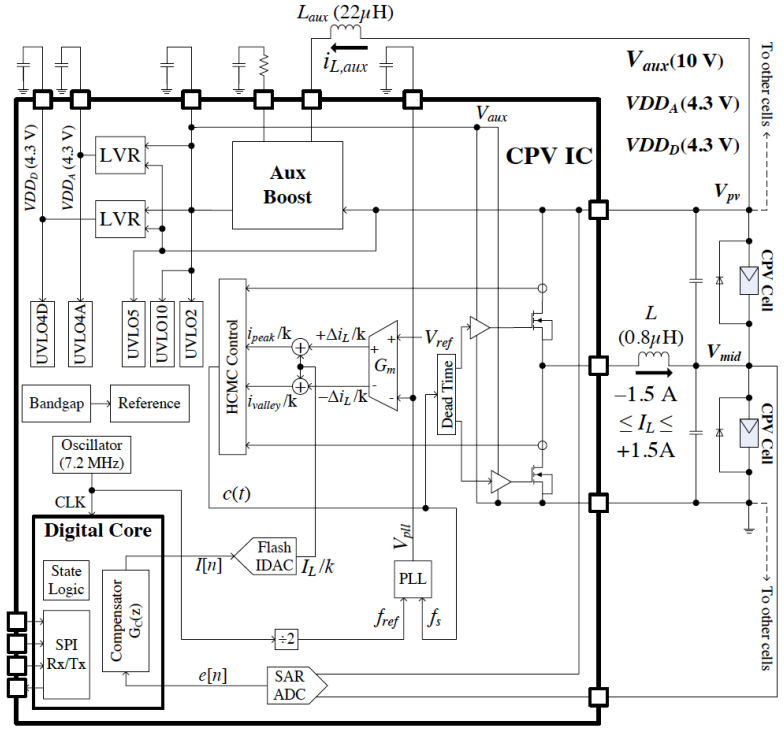


Control Scheme and IC Architecture





- Hysteretic Current-Mode Controller:
  - Analog current loop and digital voltage loop.
  - Switching frequency is imposed by a PLL.
  - No need for slope compensation.
  - Inherit current protection.
- Internal Supply Scheme:
  - On-chip boost converter (10V) to provide driver supply.
  - Two LVRs (4.3V) provide supplies for mixed-signal circuits.
  - Low-voltage start-up capability.

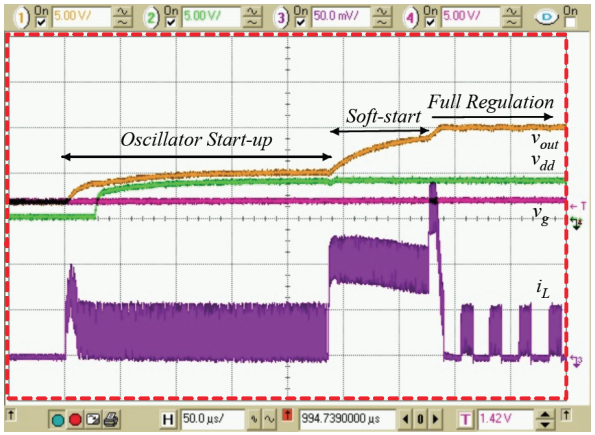


Δ-Converter Parameters

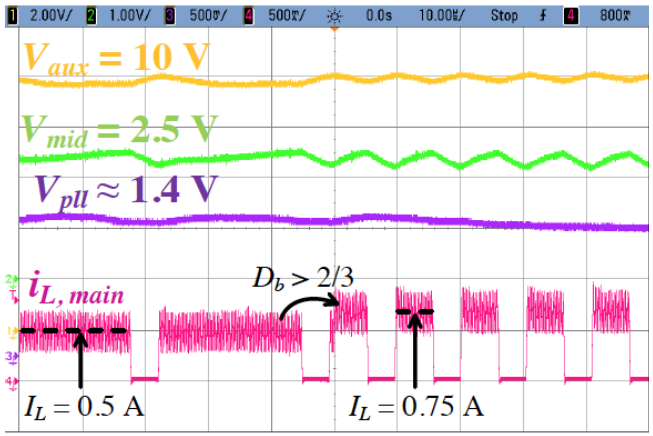
Parameter	Value	Unit
Fabrication Process	1 μm BCD	
Chip Size	2.7 × 3.7	mm^2
Peak Efficiency (Open-loop)	89	%
Closed-loop Switching Frequency, f_s	3.6	MHz
Control Mode	Hyst. Current-Mode	
Operating Voltage at V_{pv}	1.8–6.0	V
Max. Average Inductor Current, I_L	±1.5	A
Auxiliary Boost Voltage, V_{aux}	10	V
Power FET On-resistance, R_{on}	300	mΩ
Main Converter Inductance, L	0.8	μH
Auxiliary Boost Inductance, L_{aux}	22	μH

S. Zaman et.al, "A cell-level power management IC in BCD-SOI for partial power processing in Concentrating-PV systems", ISPSD 2014.

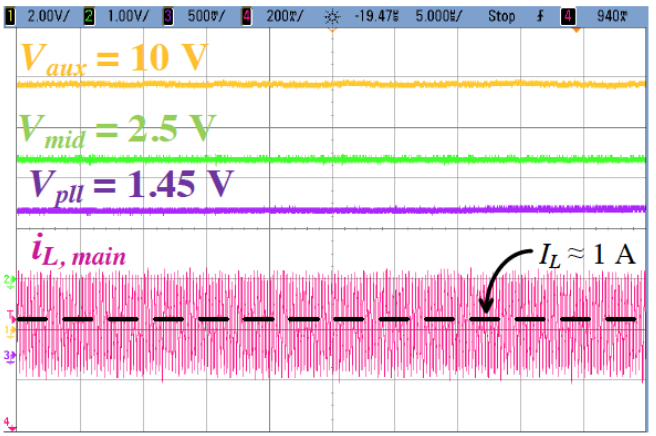
Experimental Results



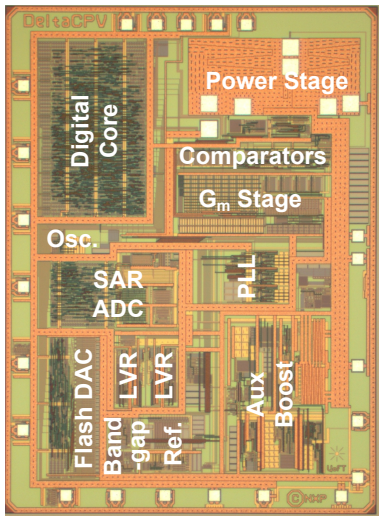
Internal supply start-up process.



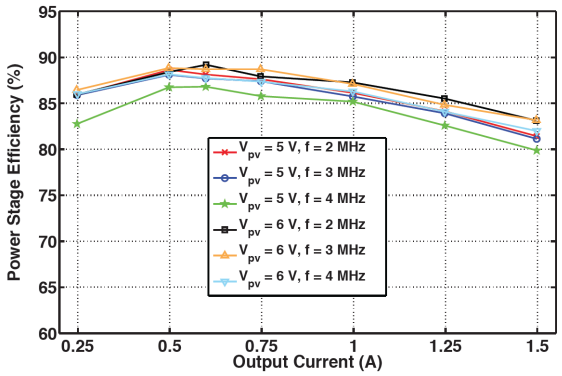
Burst-mode operation with V_{pv} = 5 V.



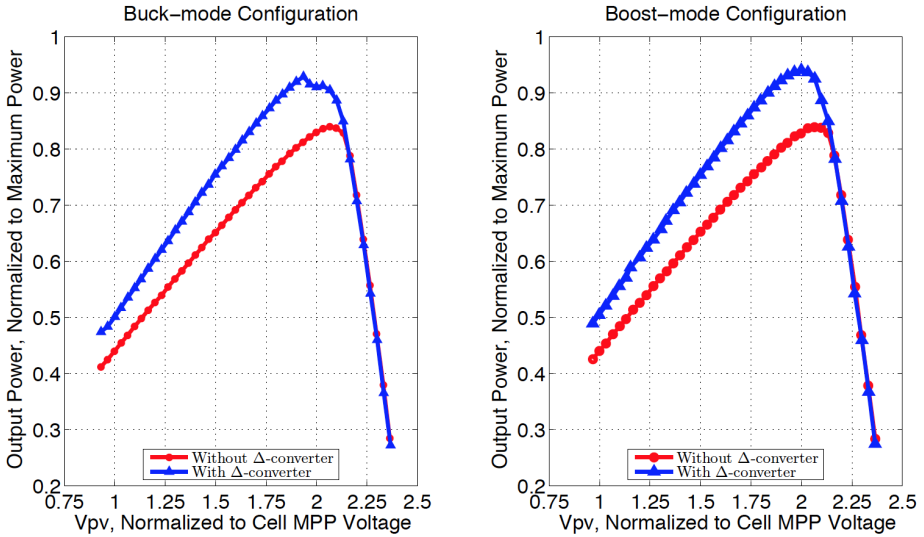
CCM operation with V_{pv} = 5 V.



Chip micrograph. The die measures 2.7×3.7 mm^2.



Open-loop converter efficiency.



Increase in PV power with Δ-converter PMIC.